WHAT IS CLAIMED IS:

1.   A method of designing a semiconductor integrated circuit, comprising the steps of:

dividing a chip of a semiconductor integrated circuit into a number of areas and providing a plurality of clock pins for each of the areas;

performing distribution of a clock signal from a clock source pin to each of the areas in a transmission form that is of high-speed and resistant to noise or the like; and

performing adjustment of a clock timing for each flip-flop in the semiconductor integrated circuit such that flip-flop-to-flip-flop data transmission can be performed in a target machine cycle,

wherein a plurality of methods having different adjustable ranges are used as methods of adjusting timing of the clock signal inputting to said flip-flop, and the flip-flops are grouped for each clock timing required by each flip-flop in said area, and said grouped flip-flops are adjusted in clock timing in accordance with requirement of each flip-flop and connected to separate clock pins.

2.   The method of designing a semiconductor integrated circuit according to claim 1, wherein in using a method of adjusting clock timing by extending wiring length, a limit is provided for the wiring length.

3.   The method of designing a semiconductor

integrated circuit according to claim 2, wherein said method is combined with another different method of adjusting timing.

4.   The method of designing a semiconductor integrated circuit according to claim 1, wherein said method provides said obtained clock timing of each flip-flop, and extracts a closed loop consisting of a plurality of signal propagation paths according to maximum delay time, minimum delay time and the target machine cycle required for data transmission along each flip-flop-to-flip-flop signal propagation path, and with respect to each flip-flop in said closed loop, selects a clock timing of each flip-flop from among clock timing that said each flip-flop can adopt such that data transmission can be performed in said target machine cycle and a cycle number required for data transmission along said closed loop.

5.   The method of designing a semiconductor integrated circuit according to claim 4, wherein said method extracts and displays a signal propagation path or a closed loop along which flip-flop-to-flip-flop data transmission can not be performed in said target machine cycle by the adjusting of said clock timing.

6.   The method of designing a semiconductor integrated circuit according to claim 4, wherein said method extracts a signal propagation path or a closed loop along which flip-flop-to-flip-flop data trans- mission can not be performed in said target machine

cycle by the adjusting of said clock timing, and with respect to the signal propagation path or the closed loop, performs modification of the delay time of flip-flop-to-flip-flop signal propagation.

7.   The method of designing a semiconductor integrated circuit according to claim 4, wherein said method determines the clock timing of each flip-flop while gradually decreasing the value of said target machine cycle, thereby determining a feasible minimum machine cycle.

8.   A system for designing a semiconductor integrated circuit, comprising the steps of:

        dividing a chip of a semiconductor integrated circuit into a number of areas and providing a plurality of clock pins for each of the areas;

        performing the distribution of a clock signal from a clock source pin to each of the areas in a transmission form that is of high-speed and resistant to noise or the like; and

        performing adjustment of clock timing for each flip-flop in the semiconductor integrated circuit such that flip-flop-to-flip-flop data transmission can be performed in a target machine cycle, comprising:

        means for calculating or means for inputting from the outside the delay time of each flip-flop-to-flip-flop signal propagation;

        means for determining clock timing of each flip-flop according to said target machine cycle;

means for outputting a method of adjusting clock timing or timing of each flip-flop;

means for realizing a given method of adjusting clock timing or timing; and

means for extracting and displaying a signal propagation path or a closed loop among flip-flops along which data transmission can not be performed within said target machine cycle.

9.   A method of designing a semiconductor integrated circuit, comprising the steps of:

providing an information file 1 including layout position information of cells, terminal-to-terminal connection relation information of cells, and wiring pattern information, clock delay designation information 2, an information file 3 including delay calculation information for calculating delay of paths, an information file 4 including clock-delay-adjusting methods, fluctuation values of clock delay caused by the adjusting methods, and clock-delay-adjusting costs by the adjusting methods, and storage means including target machine cycles (MC);

inputting data of said information files 1, 2, 3, and 4 and said storage means;

determining maximum delay time (DMAX) and minimum delay time (DMIN) required for data transmission along all flip-flop-to-flip-flop signal propagation paths;

determining a clock delay adjustable range

from the clock delay designation information input and
the clock-delay-adjusting methods capable of being
adopted by each flip-flop in said information file 4;

selecting one path, extracting a closed loop
returning from the end point flip-flop to the starting
point flip-flop of the selected path, and determining
the total delay (DLY) of delay in each path in the
closed path and a cycle number (CYC) required for data
transmission along the closed loop; and

judging whether data transmission along said
closed loop is possible in the target machine cycle or
not, and if the judgement is NG, displaying information
of the paths in the closed loop judged as the NG.

10.   The method of designing a semiconductor
integrated circuit according to claim 9,

wherein said judgement is performed by
comparing the product of the target machine cycle (MC)
input and a cycle number (CYC) required for data
transmission along said determined closed loop with the
total delay (DLY) of delay in each path in said deter-
mined closed loop,

when DLY > MC × CYC is held, NG is judged.

11.   The method of designing a semiconductor
integrated circuit according to claim 9, further
comprising the step of:

performing logic modification or packaging
modification based on the information of a path in said
displayed closed loop; and

feeding back the modification results to said information file 1.

12.   A method of designing a semiconductor integrated circuit, comprising the steps of:

providing an information file 1 including layout position information of cells, terminal-to-terminal connection relation information of cells, and wiring pattern information, clock delay designation information 2, an information file 3 including delay calculation information for calculating delay of paths, an information file 4 including clock-delay-adjusting methods, fluctuation values of clock delay caused by the adjusting methods, and clock-delay-adjusting costs by the adjusting methods, and memory including target machine cycles (MC);

inputting data of said information files 1, 2, 3, and 4 and said memory;

determining maximum delay time (DMAX) and minimum delay time (DMIN) required for data trans-mission along all flip-flop-to-flip-flop signal propagation paths;

determining a clock delay adjustable range from the clock delay designation information input and the clock-delay-adjusting method capable of being adopted by each flip-flop in said information file 4;

selecting one path, extracting a closed loop returning from the end point flip-flop to the starting point flip-flop of the selected path, and determining

the total delay (DLY) of delay in each path in the closed loop and a cycle number (CYC) required for data transmission along the closed loop; and

judging whether the data transmission along said closed loop is possible in the target machine cycle or not, and if the judgement is OK, setting a clock-delay-adjusting range permitting data trans-mission to each flip-flop so as to satisfy a predeter-mined restraint for each path.

13.   The method of designing a semiconductor integrated circuit according to claim 12,

wherein the step of setting said clock-delay-adjusting range satisfies the following restraints for each path, and sets the clock-delay-adjusting range of each flip-flop within said determined clock delay adjustable range of each flip-flop.

$MC \times CYC (PATH) - CLK (S.FF) MAX + CLK (E.FF) MIN > DMAX$

$MC \times (CYC (PATH) - 1) - CLK (S.FF) MIN + CLK (E.FF) MAX < DMIN$,

wherein CYC (PATH): the cycle number required for data transmission along the path concerned,

CLK (S.FF) MIN, CLK (S.FF) MAX: the clock-delay-adjusting range of the starting point flip-flop, and

CLK (E.FF) MIN, CLK (E.FF) MAX: the clock-delay-adjusting range of the end point flip-flop.

14.   The method of designing a semiconductor

integrated circuit according to claim 12, further
comprising the step of outputting the clock-delay-
adjusting range set to each flip-flop to the clock
delay setting information file, when the setting of
clock delay to all paths is completed.

15.   A method of designing a semiconductor
integrated circuit, comprising the steps of:

inputting each flip-flop-to-flip-flop path
delay and a target machine cycle obtained in the stages
of physical design and packaging design, and with
respect to a path in which the path delay is not less
than the target machine cycle;

extracting a closed loop including the path;
and

adjusting the timing of a clock signal of
each flip-flop so as to permit data transmission in a
cycle number required for the closed loop,

wherein a plurality of methods different in
the adjustable range of clock timing are used as the
methods of adjusting the timing of a clock signal to
each flip-flop, and a path along which data trans-
mission is impossible in said target machine cycle or a
closed loop including the path is displayed in order to
be modified.